DAC8555EVM User's Guide

This user's guide describes the characteristics, operation and use of the DAC8555 Evaluation Module (EVM). It covers all matters related to proper use and configuration of this EVM along with the devices that it supports. The physical printed circuit board (PCB) layout, schematic diagram and circuit descriptions are also included. For a more detailed description of the DAC8555, see the product data sheet available from the Texas Instruments web site at http://www.ti.com. Additional support documents are listed in the section of this guide entitled ***Related Documentation from Texas Instruments***. Throughout this document, the acronym *EVM* and the phrases *evaluation module* and *demonstration board* are synonymous with the DAC8555EVM.

Contents

List of Figures

List of Tables

1 Overview

This section gives a general overview of the DAC8555EVM and describes some of the factors that must be considered when using this demonstration board.

1.1 Features

The DAC8555EVM is a simple evaluation module designed for a quick and easy way to evaluate the functionality and performance of the high-resolution, quad-channel, serial input DAC8555 digital-to-analog converter (DAC). This EVM features a serial interface to communicate with any host microprocessor or TI DSP-based system.

1.2 Power Requirements

This subsection describes the power requirements for this device.

1.2.1 Supply Voltage

The DC power supply requirement for the digital section (V_{DD}) of this EVM is typically +5V connected to the J5-1 terminal or via the J3-10 terminal (when plugged in with another EVM board or interface card) and is referenced to ground through the J5-2 and J3-5 terminals. The DC power supply requirements for the analog section of this EVM are: V_{CC} and V_{SS} range from +15.75V to –15.75V (maximum), connecting through J1-3 and J1-1 respectively, or through terminals J3-1 and J3-2. The $+5V_A$ connects through terminals J5-3 or J3-3, and the $+3.3V_A$ connects through terminal J3-8. All of the analog power supplies are referenced to analog ground through terminals J1-2 and J3-6.

The analog power supply for the device under test, U1, can be powered by either $+5V_A$ or $+3.3V_A$ by selecting the proper position of jumper JMP7. This configuration allows the DAC8555 analog section to operate from either supply power while the I/O and digital section are powered by +5V, V_{DD}.

The V_{CC} supply source is primarily used to provide the positive rail of the external output op amp, U2, the reference chip, U3 and the reference buffer, U4. The negative rail of the output op amp, U2, can be selected between V_{SS} and AGND via jumper JMP10. The external op amp is installed as an option to provide output signal conditioning or to boost capacitive load drive, or for other desired output mode requirements.

CAUTION

To avoid potential damage to the EVM board, be sure that the correct cables are connected to their respective terminals as labeled on the EVM board. Stresses above the maximum listed voltage ratings may cause permanent damage to the device.

1.2.2 Reference Voltage

The +5V precision voltage reference is provided to supply the external voltage reference for the DAC through the REF02 (U3) via jumper JMP8, by shorting pins 1 and 2. The reference voltage goes through an adjustable 100kΩ potentiometer, R15, in series with 20kΩ, R16, to allow the user to adjust the reference voltage to its desired settings. The voltage reference is then buffered through U4A as seen by the device under test. The test points TP2, TP3 and TP4 are also provided, as well as J4-18 and J4-20, in order to allow the user to connect another external reference source if the onboard reference circuit is not desired. The external voltage reference should not exceed +5V DC.

The REF02 precision reference is powered by V_{CC} (+15V) through either terminal J1-3 or J3-1.

CAUTION

When applying an external voltage reference through TP2 or J4-20, make sure that it does not exceed +5V maximum. External voltage references in excess of +5V can permanently damage the DAC8555 being tested (U1).

1.3 EVM Basic Functions

The DAC8555EVM is designed to provide a demonstration platform for testing certain operational characteristics of the DAC8555 digital-to-analog converter. Functional evaluation of the DAC8555 can be accomplished with the use of any microprocessor, TI DSP or some sort of waveform generator.

Headers J2A (top side) and J2B (bottom side) are pass-through connectors provided to interface a host processor or waveform generator with the DAC8555EVM using a custom-built cable. These connectors enable the control signals and data to pass between the host and the device.

A mating adapter interface card (5-6k adapter interface) is also available to fit with TI's TMS320C5000™ and TMS320C6000™ DSP Starter Kits (DSKs). This card resolves most of the trouble involved with building a custom cable. Additionally, there is also an MSP430-based platform (HPA449) that uses the MSP430F449 microprocessor, to which this EVM can connect and interface as well. For more details or information regarding the 5-6k adapter interface card or the HPA449 platform, please contact your Texas Instruments representative, visit the TI web site or email the Data Converter Applications Support Team at **dataconvapps@list.ti.com**.

The DAC outputs can be monitored through the selected pins of the J4 header connector. All outputs can be switched through their respective jumpers—JMP11, JMP12, JMP13 and JMP14—for the purpose of stacking. Stacking allows a total of eight DAC channels to be used, provided the $\overline{\text{SYNC}}$ signals are unique for each EVM board stacked.

In addition, the option of selecting one DAC output that can be fed to the noninverting side of the output op amp, U2, is also possible by using a jumper across the selected pins of J4. The output op amp (U2) must first be correctly configured for the desired waveform characteristic. For more information, refer to Section 3 of this user's guide.

A block diagram of the EVM is shown in Figure 1.

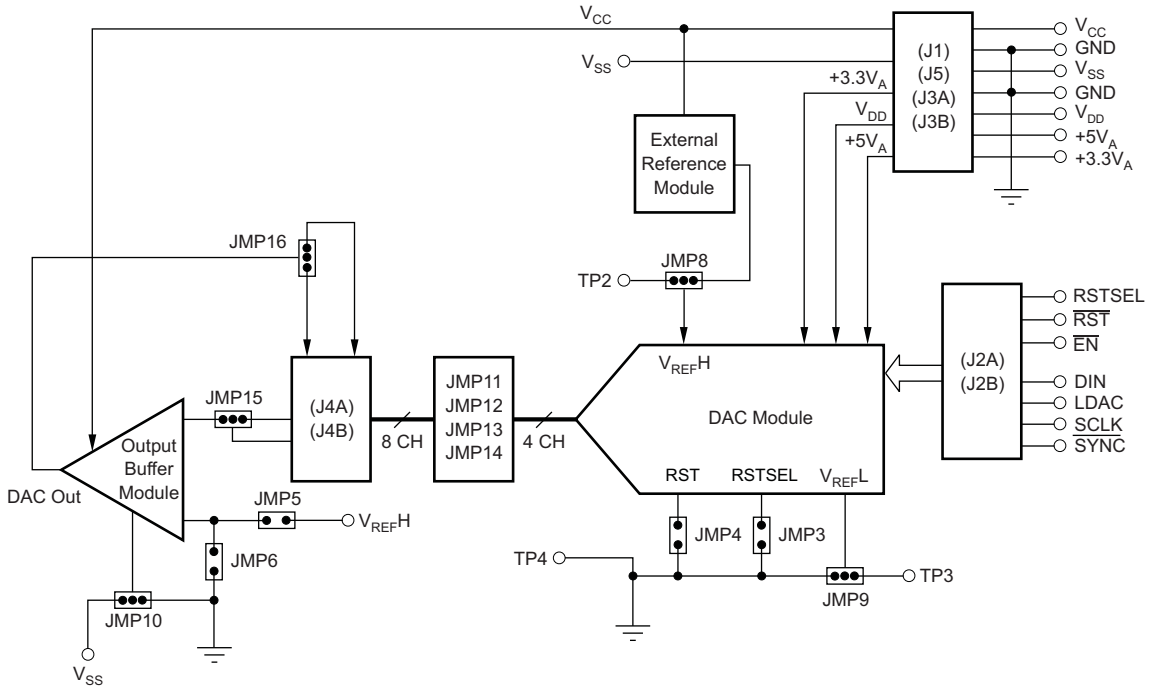


Figure 1. DAC8555EVM Functional Block Diagram

1.3.1 Related Documentation from Texas Instruments

The following documents provide information regarding Texas Instrument integrated circuits used in the assembly of the DAC8555EVM. The latest revisions of these documents are available from the TI web site at http://www.ti.com.

Data Sheet	Literature Number
DAC8555	SLAS475
REF02	SBVS003
OPA627	SBOS165
OPA2132	SBOS054

2 PCB Design and Performance

This section discusses the layout design of the DAC8555EVM PCB, describing the physical and mechanical characteristics of the EVM as well as a brief description of the demonstration board test performance procedures performed. The list of components used in this evaluation module is also included.

2.1 PCB Layout

The DAC8555EVM is designed to preserve the performance quality of the DAC8555, the device under test (DUT), as specified in the data sheet. In order to take full advantage of the EVM capabilities, use care during the schematic design phase to properly select the right components and to build the circuit correctly. The circuit design should include adequate bypassing, identifying and managing the analog and digital signals, and understanding the components' electrical and mechanical attributes.

The primary design concerns during the layout process are optimal component placement and proper signal routing. Place the bypass capacitors as close as possible to the device pins, and properly separate the analog and digital signals from each other. In the layout process, carefully consider the placement of the power and ground planes. A solid plane is ideal, but because of its greater cost, a split plane can sometimes be used satisfactorily. When considering a split plane design, analyze the component placement and carefully split the board into its analog and digital sections starting from the DUT. The ground plane plays an important role in controlling the noise and other effects that otherwise contribute to the error of the DAC output. To ensure that the return currents are handled properly, route the appropriate signals only in their respective sections, meaning that the analog traces should only lay directly above or below the analog section and the digital traces in the digital section. Minimize trace length, but use the largest possible trace width allowable within the design. These design practices are illustrated in Figure 2 through Figure 8.

The DAC8555EVM board is constructed on a four-layer PCB using a copper-clad FR-4 laminate material. The PCB has a dimension of 43,1800mm (1.7000in) by 82,5500mm (3.2500in), and the board thickness is 1,5748mm (0.062in). Figure 3 through Figure 7 show the individual artwork layers.

Note: Board layouts are not to scale. These are intended to show how the board is laid out; they are not intended to be used for manufacturing DAC8555EVM PCBs.

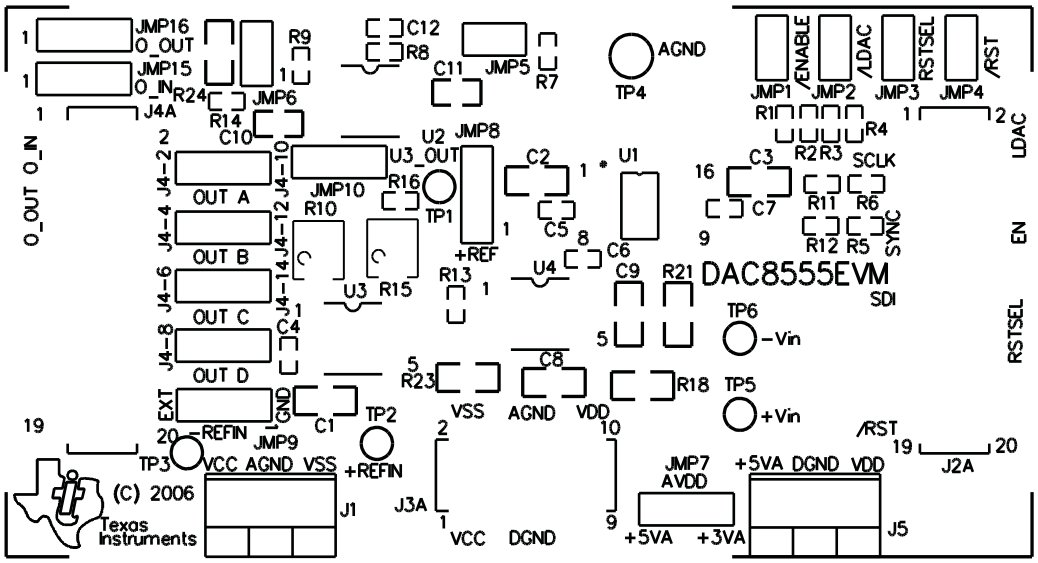


Figure 2. DAC8555EVM PCB—Top Silkscreen Image

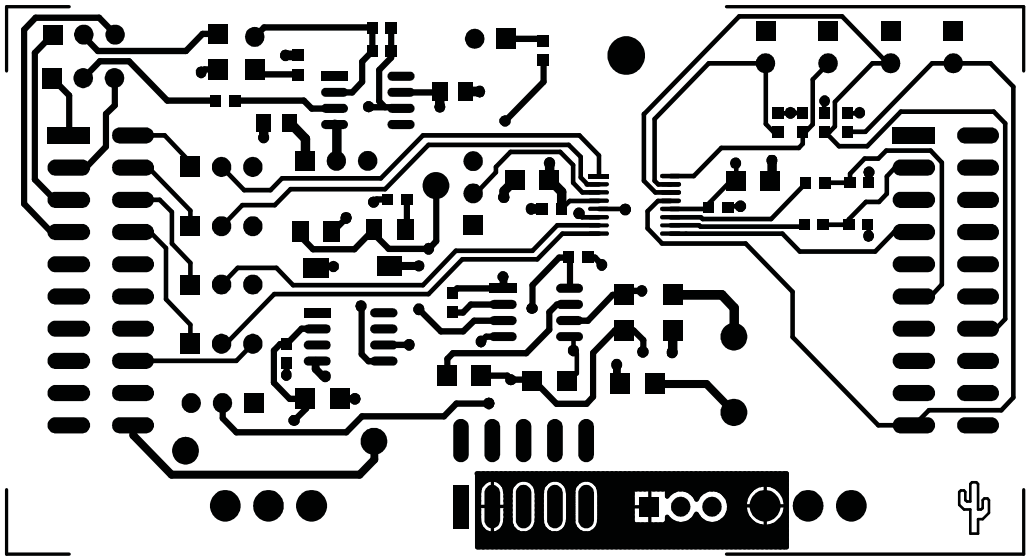


Figure 3. DAC8555EVM PCB—Layer 1 (Top Signal Layer)

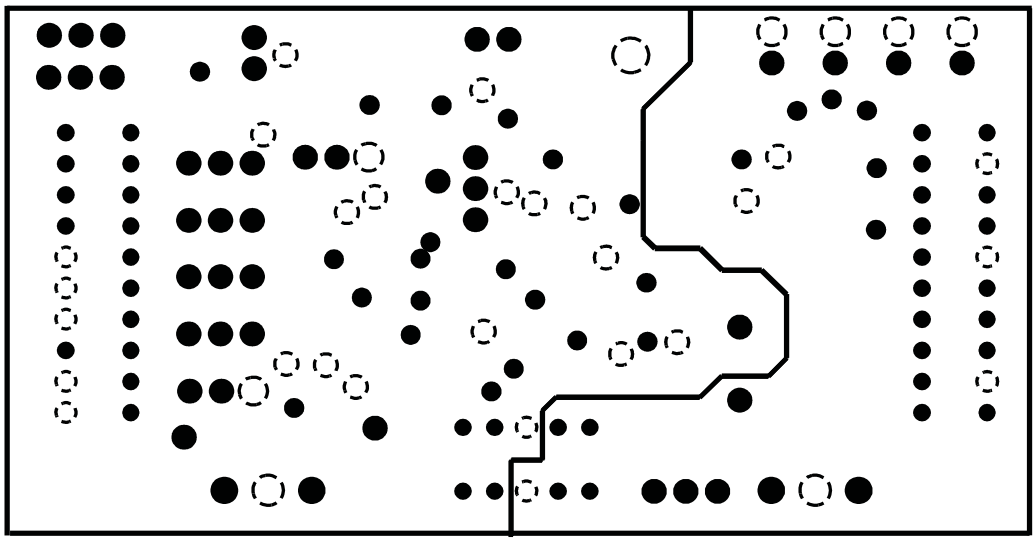


Figure 4. DAC8555EVM PCB—Layer 2 (Ground Plane)

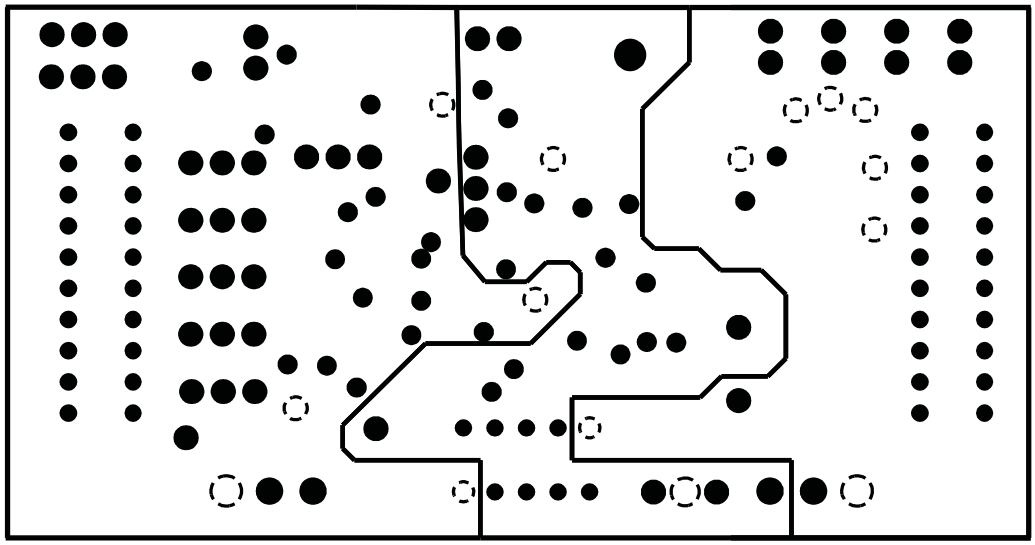


Figure 5. DAC8555EVM PCB—Layer 3 (Power Plane)

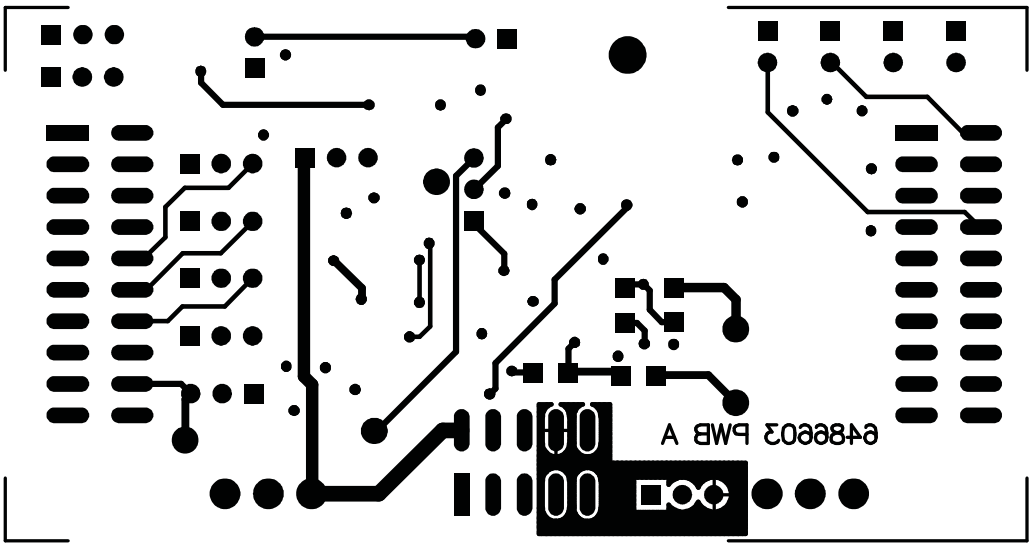


Figure 6. DAC8555EVM PCB—Layer 4 (Bottom Signal Layer)

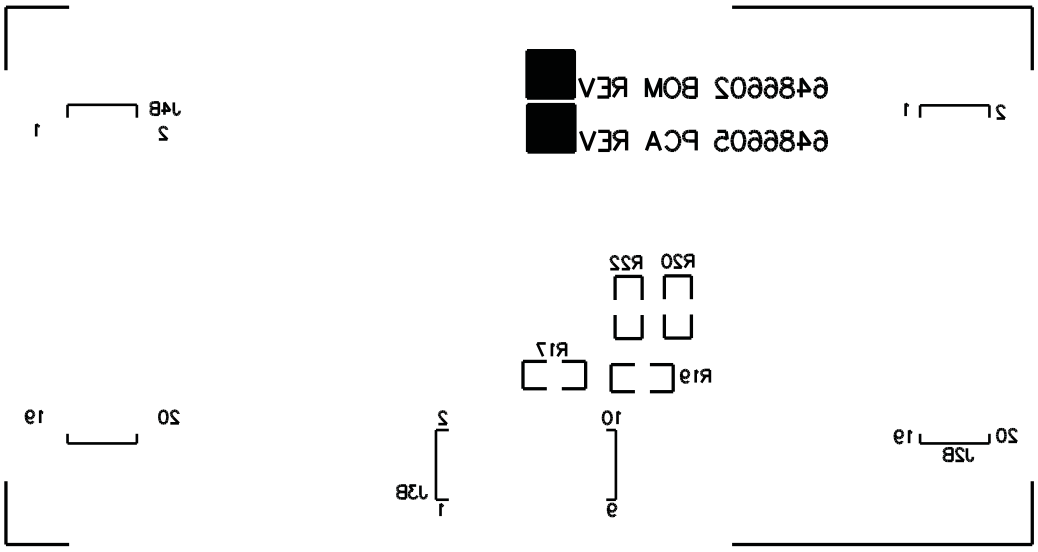


Figure 7. DAC8555EVM PCB—Bottom Silkscreen Image

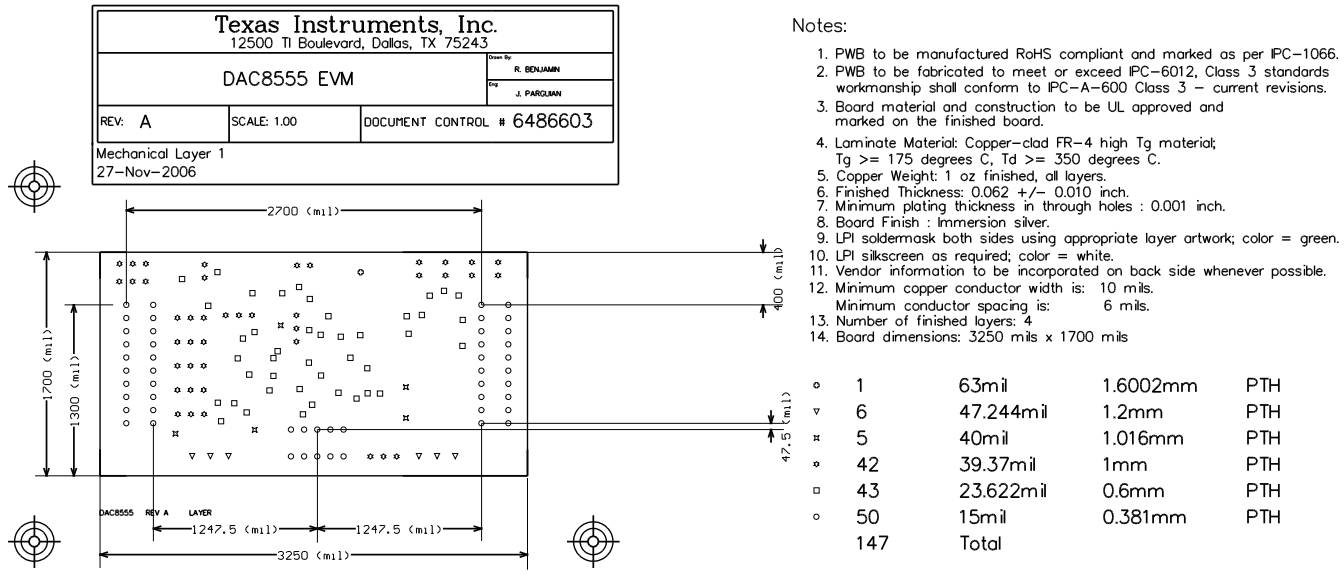


Figure 8. DAC8555EVM—Drill Drawing

2.2 EVM Performance

The EVM performance test is executed using a high-density DAC bench test board, an Agilent 3458A digital multimeter and a PC running LabVIEW™ software. The EVM board is tested for linearity for all codes between 485 and 64741. The DUT is then allowed to settle for 1ms before the meter is read. This process is repeated for all codes to generate the measurements for INL and DNL.

Results of the DAC8555EVM tests are shown in Figure 9 through Figure 12.

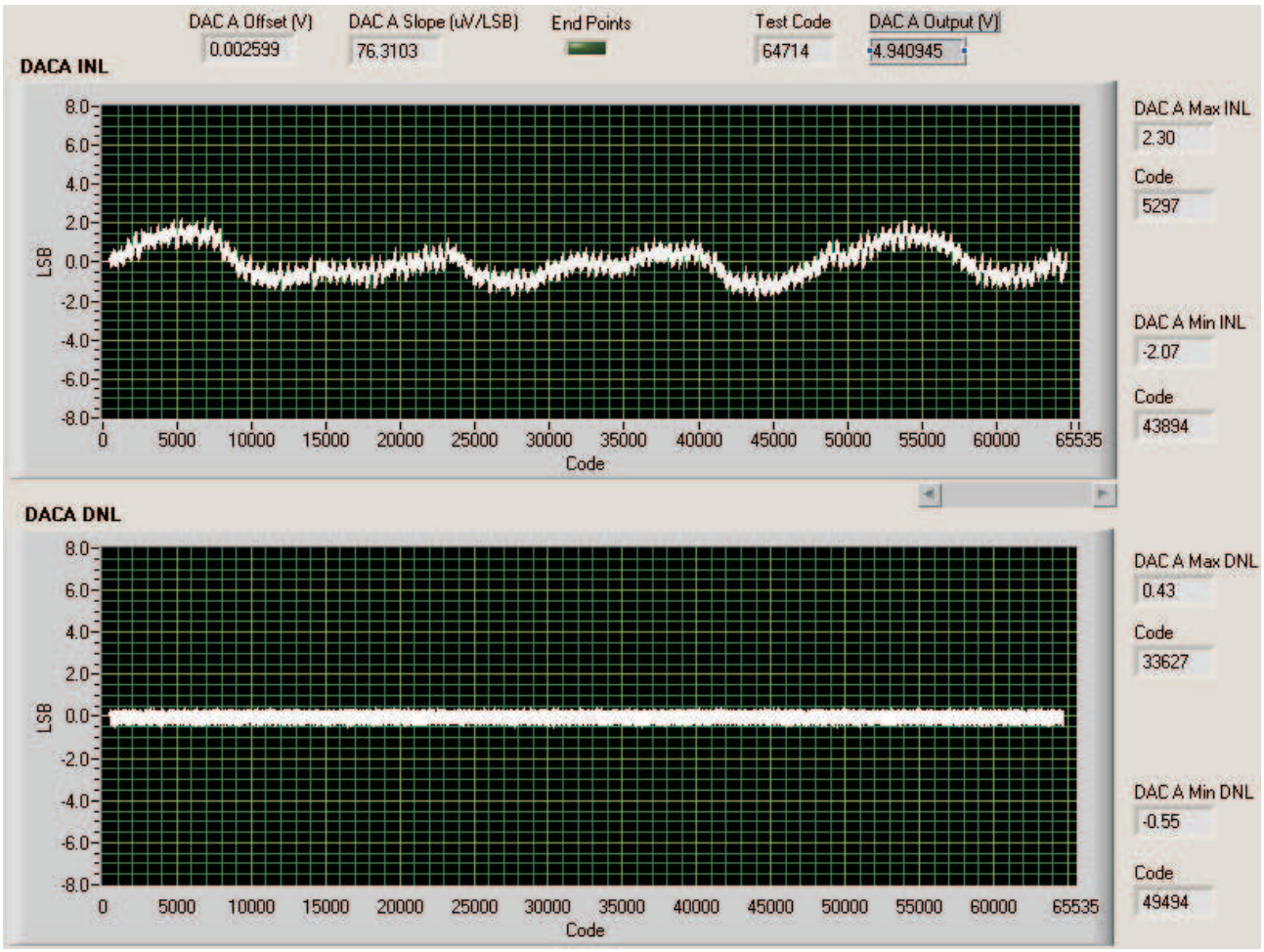


Figure 9. INL and DNL Characterization Graph of DAC A

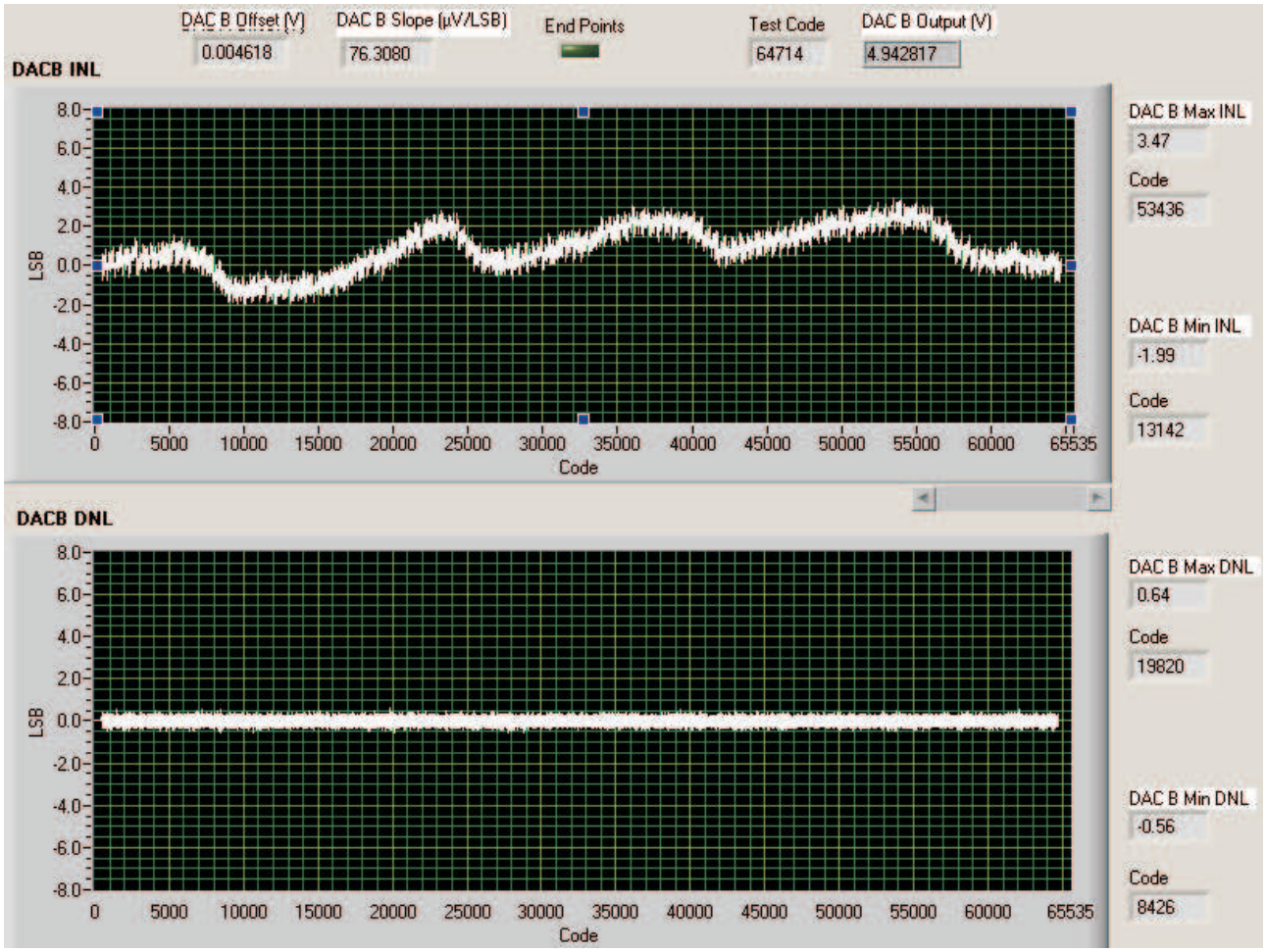


Figure 10. INL and DNL Characterization Graph of DAC B

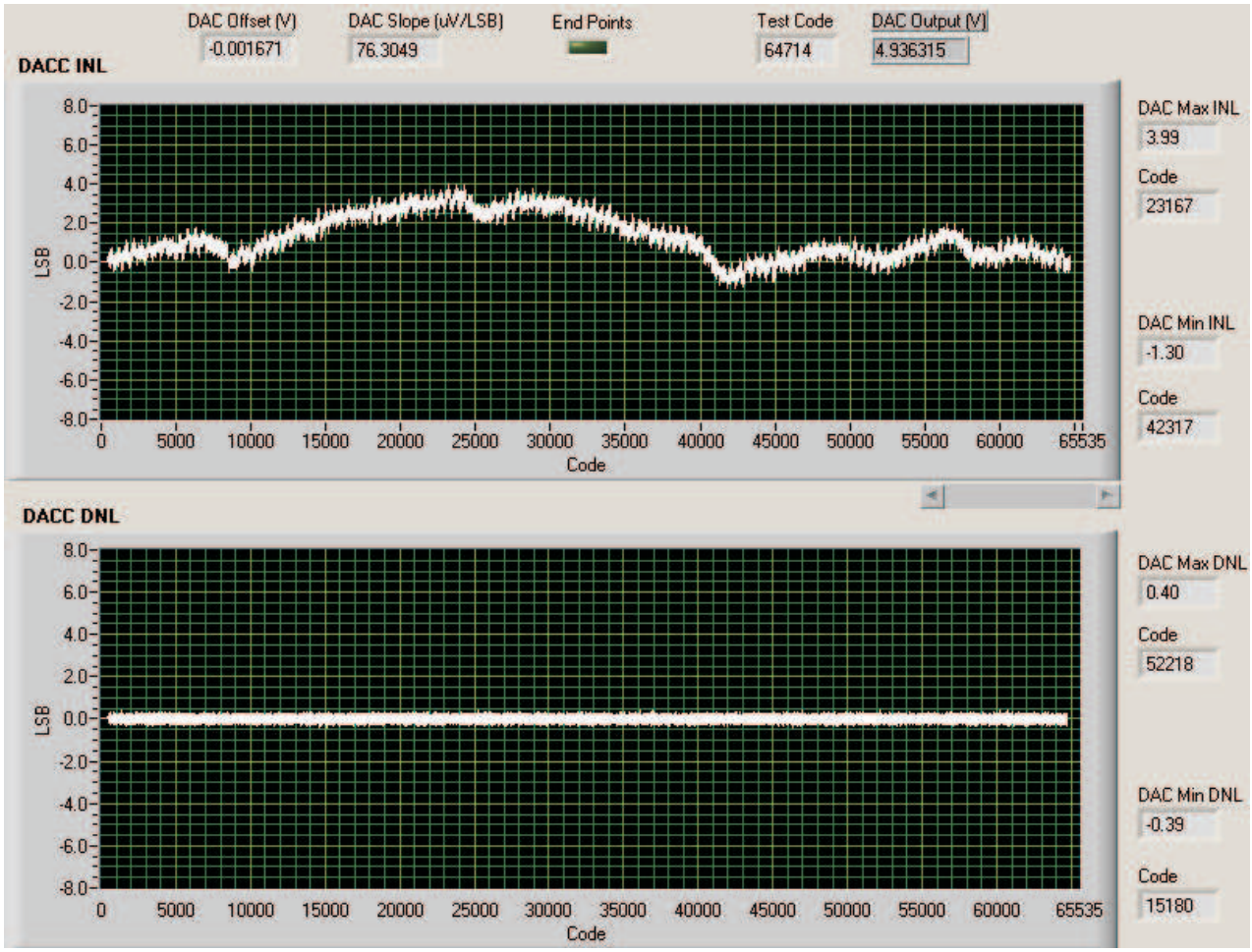


Figure 11. INL and DNL Characterization Graph of DAC C

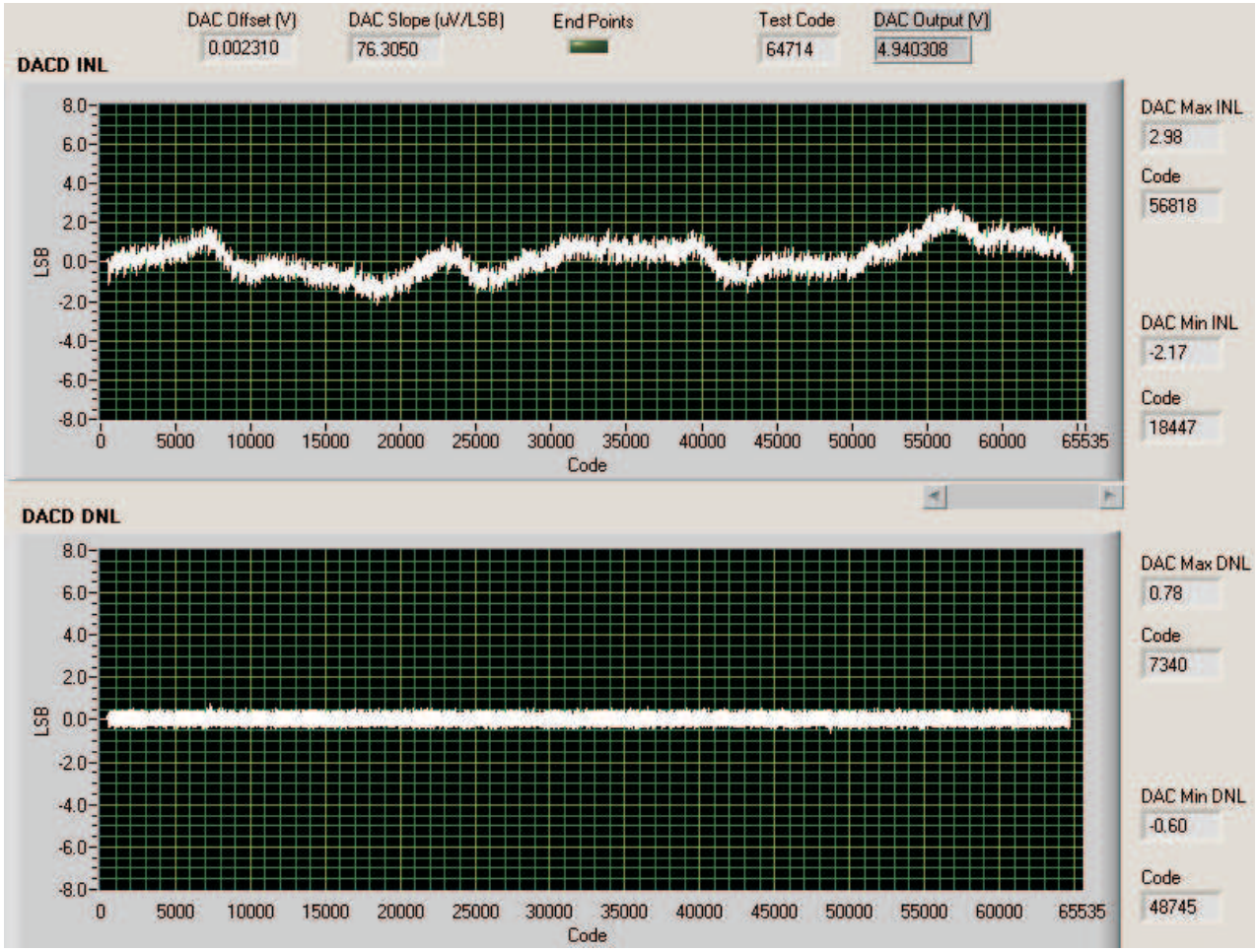


Figure 12. INL and DNL Characterization Graph of DAC D

2.3 Bill of Materials

The parts list, showing the components used in the assembly of the DAC8555EVM, is given in Table 1.

Table 1. DAC8555EVM Parts List

ITEM	QTY PER BOARD	Ref Des	MFR	MFR PART NUMBER	DESCRIPTION
1	4	R11–R14	Panasonic	ERJ-3GEY0R00V	Chip Resistor, 0Ω, 1/10W, 0603
2	1	R24	Panasonic	ERJ-8GEYJ101V	Chip Resistor, 100Ω, 1/4W, 1206
Not Installed	2	R5, R6	Panasonic	ERJ-3GEYJ302V	Chip Resistor, 3kΩ, 1/10W, 0603
3	7	R1–R4, R7, R8, R9	Panasonic	ERJ-3EKF1002V	Chip Resistor, 10kΩ, 1/16W, 0603
4	1	R16	Panasonic	ERJ-3EKF2002V	Chip Resistor, 20kΩ, 1/16W, 0603
5	1	R10	Bourns	3214W-1-203E	Series 5T Pot., 20kΩ, BOURNS_32X4W
6	1	R15	Bourns	3214W-1-104E	Series 5T Pot., 100kΩ, BOURNS_32X4W
Not Installed	7	R17–R23	Panasonic		Chip Resistor, 1/4W 1206
7	1	C12	TDK	C1608C0G1H102J	Multilayer Ceramic Capacitor, 1nF, 0603 C0G
8	4	C4–C7	TDK	C1608X7R1E104K	Multilayer Ceramic Capacitor, 0.1μF, 0603 X7R
9	2	C10, C11	TDK	C2012X7R1E105K	Multilayer Ceramic Capacitor, 1μF, 0805 X7R
10	3	C1, C2, C3	TDK	C3216X7R1C106M	Multilayer Ceramic Capacitor, 10μF, 1206 X7R
Not Installed	2	C8, C9	TDK		Multilayer Ceramic Capacitor, 1206
11	1	U1	Texas Instruments	DAC8555IPW	16-bit, Quad Voltage Output, Serial Input DAC, TSSOP-16
12	1	U2	Texas Instruments	OPA627AU	8-SOP(D) Precision Op Amp
13	1	U3	Texas Instruments	REF02AU	+5V, 8-SOP(D) Precision Voltage Reference
14	1	U4	Texas Instruments	OPA2132UA	8-SOP(D) Dual Precision Op Amp
Not Installed	2	J1, J5	On-Shore Technology	ED555/3DS	3-Pin Terminal Connector
15	2	J2A, J4A	Samtec	TSM-110-01-L-DV-P	SMT Header, 10x2x0.1, 20-pin, .025in^2
16	1	J3A	Samtec	TSM-105-01-L-DV-P	SMT Header, 5x2x0.1, 10-pin, .025in^2
17	2	J2B, J4B	Samtec	SSW-110-22-F-D-VS-K	SMT Socket, 10x2x0.1, 20-pin, .025in^2
18	1	J3B	Samtec	SSW-105-22-F-D-VS-K	SMT Socket, 5x2x0.1, 10-pin, .025in^2
19	6	JMP1–JMP6	Samtec	TSW-102-07-G-S	2-position Jumper_ .1in spacing
20	10	JMP7–JMP16	Samtec	TSW-103-07-G-S	3-position Jumper_ .1in spacing
21	1	TP4	Keystone Electronics	5011	Testpoint, Large-Loop
Not Installed	5	TP1, TP2, TP3, TP5, TP6	Keystone Electronics	5000	Testpoint, Mini-Loop
22	16	N/A	Samtec	SNT-100-BK-G-H	Shorting Block

3 EVM Operation

This section covers the operation of the EVM in detail, in order to provide guidance to the user in evaluating the onboard DAC as well as how to interface the EVM to a specific host processor. Refer to the DAC8555 datasheet for information about its serial interface and other related topics. The EVM board is factory-tested and configured.

3.1 Default Settings

The EVM is set to its factory default configuration as described in Table 2 to operate in 5V mode.

Table 2. Factory Default Jumper Settings

Reference	Jumper Position	Function
JMP1	CLOSE	$\overline{\text{ENABLE}}$ pin is tied to DGND
JMP2	CLOSE	LDAC pin is tied to DGND. Software LDAC is used.
JMP3	CLOSE	RSTSEL pin is tied to DGND.
JMP4	OPEN	$\overline{\text{RST}}$ pin is tied to V_{DD}.
JMP5	OPEN	$V_{REF}H$ is not routed to the inverting input of the op amp for voltage offset with gain of 2 output.
JMP6	OPEN	Output op amp U2 is not configured for a gain of 2.
JMP7	1-2	Analog supply for the DAC8555 is $+5V_A$.
JPM8	1-2	Onboard external buffered reference U3 is routed to $V_{REF}H$.
JMP9	1-2	$V_{REF}L$ is tied to AGND.
JMP10	1-2	Negative supply rail of U2 op amp is supplied with V_{SS}.
JMP11	1-2	DAC output A ($V_{OUT}A$) is routed to J4-2.
JMP12	1-2	DAC output B ($V_{OUT}B$) is routed to J4-4.
JMP13	1-2	DAC output C ($V_{OUT}C$) is routed to J4-6.
JMP14	1-2	DAC output D ($V_{OUT}D$) is routed to J4-8.
JMP15	1-2	J4-1 is connected to the noninverting input of the output op amp U2.
JMP16	1-2	J4-5 is connected to the output of the op amp U2.

3.2 Host Processor Interface

The host processor drives the DAC. Thus, proper DAC operation depends on a successful configuration between the host processor and the EVM board. In addition, properly written code is also required to operate the DAC.

As discussed earlier, a custom cable can be made specific to the host interface platform. The EVM allows interface to the host processor through header connector J2 for the serial control signals and the serial data input. The output can be monitored through header connector J4.

An interface adapter card is also available for specific TI DSP DSKs as well as an MSP430-based microprocessor (see Section 1.3 of this manual). Using the interface card alleviates the tedious task of building customized cables and allows easy configuration of a simple evaluation system.

The DAC8555 interfaces with any host processor capable of handling SPI protocols or the popular TI DSPs. For more information regarding the DAC8555 data interface, please refer to the DAC8555 datasheet.

3.3 EVM Stacking

Stacking multiple EVMS is possible if there is a need to evaluate two DAC8555s, yielding a total of eight output channels. A maximum of two EVMs can be stacked since the output terminal, J4, dictates the number of DAC channels that can be connected without colliding. Table 3 shows how the DAC output channels are mapped into the output terminal, J4, with respect to the jumper positions of JMP11, JMP12, JMP13, and JMP14.

Table 3. DAC Output Channel Mapping

Reference	Jumper Position	Function
JMP11	1-2	DAC output A ($V_{OUT}A$) is routed to J4-2.
	2-3	DAC output A ($V_{OUT}A$) is routed to J4-10.
JMP12	1-2	DAC output B ($V_{OUT}B$) is routed to J4-4.
	2-3	DAC output B ($V_{OUT}B$) is routed to J4-12.
JMP13	1-2	DAC output C ($V_{OUT}C$) is routed to J4-6.
	2-3	DAC output C ($V_{OUT}C$) is routed to J4-14.
JMP14	1-2	DAC output D ($V_{OUT}D$) is routed to J4-8.
	2-3	DAC output D ($V_{OUT}D$) is routed to J4-16.

In order to allow exclusive control of each EVM, different $\overline{\text{SYNC}}$ signals must be selected for each DAC8555. This difference is not easily accomplished as it involves hardware alterations. The EVM board that sits on the bottom of the stack can use the $\overline{\text{SYNC}}$ signal coming from J2B-7. The pin of J2A-7 can be cut so that the $\overline{\text{SYNC}}$ signal coming from the bottom EVM board in the stack does not pass through. The EVM board that sits on top can use the CNTL signal coming from J2-1. The signal of J2-1 must be jumpered across to J2-7 of the EVM board that sits on the top of the stack. The LDAC, $\overline{\text{SYNC}}$ and $\overline{\text{ENABLE}}$ control signals are shared. The DAC8555 only responds when the correct $\overline{\text{SYNC}}$ signal is generated.

The raw outputs of the DAC can be probed through the even numbered pins of J4, the output terminal, which also provides mechanical stability when stacking or plugging into any interface card. In addition, it provides easy access for monitoring up to eight DAC channels when stacking two EVMs together.

3.4 Output Op Amp

The DAC8555EVM includes an optional signal conditioning circuit for the DAC output through an external operational amplifier, U2. The output op amp is set to unity gain configuration by default. Only one DAC output channel can be monitored at any given time. JMP15 selects which pin of J4 is the input. Either J4-1 or J4-3 can be used as the op amp signal input. The default setting for JMP15 selects J4-1. A shorting jumper can be placed between one of the DAC outputs and the op amp input. For example, a jumper across J4-1 and J4-2 places the DAC A output as the input for the op amp if board jumpers are in the default position. If JMP15 is in the alternate position, then a shorting block between J4-3 and J4-2 makes the DAC B output the input to the op amp.

The output of U2 passes through JMP16. In the default position, the output connects to J4-5. When JMP16 is in the alternate position, the output from U2 connects to J4-7. The output can be monitored from, or passed to, another device from the J4 connector.

The jumper arrangement of JMP15 and JMP16 connecting to J4 allows U2 to be used in the stacked board arrangement discussed above in Section 3.3.

The following subsections describe the different configurations of the output amplifier, U2.

3.4.1 Unity Gain Output

The buffered output configuration can be used to prevent loading of the DAC8555, though it may add some slight distortion because of the feedback resistor and capacitor. The feedback circuit can be altered by simply desoldering R8 and C12 and replacing them with components of desired value. If desired, R8 and C12 can be removed altogether by replacing R8 with a 0Ω resistor.

Table 4 shows the jumper setting for the unity gain configuration of the DAC external output buffer in unipolar or bipolar mode.

Table 4. Unity Gain Output Jumper Settings

Reference	Jumper Setting		Function
	Unipolar	Bipolar	
JMP5	Open	Open	Disconnect $V_{REF}H$ from the inverting input of the op amp.
JMP10	2-3	1-2	Supplies V_{SS} to the negative rail of the op amp or ties it to AGND.
JMP6	Open	Open	Disconnect negative input of op amp from the gain resistor, R9.

3.4.2 Output Gain of 2

There are two types of configurations that will yield an output gain of 2, depending on the setup of jumpers JMP5 and JMP6. These configurations allow the user to choose whether the DAC output will use $V_{REF}H$ as an offset. Table 5 shows the proper jumper settings of the EVM for the DAC8555 output gain of 2.

Table 5. Output Gain of 2 Jumper Settings

Reference	Jumper Setting		Function
	Unipolar	Bipolar	
JMP5	Close	Close	Inverting input of the output op amp U2 is connected to $V_{REF}H$ for use as its offset voltage with a gain of 2. JMP6 must be open.
	Open	Open	$V_{REF}H$ is disconnected from the inverting input of the output op amp U2. JMP6 must be closed.
JMP10	2-3	1-2	Supplies power, V_{SS}, to the negative rail of op amp U2 for bipolar mode, or ties it to AGND for unipolar mode.
JMP6	Close	Close	Configures op amp U2 for a gain of 2 output without a voltage offset. JMP5 must be open.
	Open	Open	Inverting input of op amp U2 is disconnected from the gain resistor, R9. JMP5 must be closed.

3.4.3 Capacitive Load Drive

It may be required to drive a wide range of capacitive loads. However, under certain conditions, all op amps may become unstable, depending on the op amp configuration, gain, and load value. These factors are just few of the issues that can affect op amp stability and should be considered during implementation.

In unity gain configuration, the OPA627 op amp (U2) performs very well with very large capacitive loads. Increasing the gain enhances amplifier ability to drive even more capacitance, and adding a load resistor even improves the capacitive load drive capability.

Table 6 shows the jumper setting configuration for a capacitive load drive.

Table 6. Capacitive Load Drive Output Jumper Settings

Reference	Jumper Setting		Function
	Unipolar	Bipolar	
JMP5	Open	Open	$V_{REF}H$ is disconnected from the inverting input of the output op amp U2.
JMP10	2-3	1-2	Supplies power, V_{SS}, to the negative rail of op amp U2 for bipolar mode, or ties it to AGND for unipolar mode.
JMP6	Open	Open	Capacitive load drive output of DAC is routed to pin 2 of JMP6 and may be used as the output terminal.

3.5 Optional Signal Conditioning Op-Amp (U4B)

One half of the OPA2132 dual package op amp (U4) is used for reference buffering (U4A), while the other half is unused. This unused op amp (U4B) is left for whatever op amp circuit application the user desires to implement. The 1206 footprint for the resistors and capacitors surrounding the U4B op amp are not populated and are made available for easy configuration. Test points TP5 and TP6 are not installed, so it is up to the user on how to connect the (±) input signals to this op amp. No test point has been made available for the output because of space restrictions, but a wire can be soldered to the output of the op amp via an unused component pad that connects to it. The op amp circuit can be configured by populating the corresponding components to those that match the circuit design while leaving all other unused component footprints unpopulated.

3.6 Jumper Settings

Table 7 shows the function of each specific jumper setting of the EVM.

Table 7. Jumper Settings and Functions

Reference	Jumper Setting(1)	Function
JMP1		$\overline{\text{ENABLE}}$ pin is set high through pull-up resistor R1. $\overline{\text{ENABLE}}$ can be driven by GPIO2, J2-8.
		$\overline{\text{ENABLE}}$ pin is set low and DAC is enabled.
JMP2		LDAC pin is set high through pull-up resistor R2. LDAC can be driven by GPIO0, J2-2.
		LDAC pin is set low and DAC update is accomplished via software.
JMP3		RSTSEL pin is set high through pull-up resistor R3. RSTSEL can be driven by GPIO4, J2-14.
		RSTSEL pin is set low.

(1) Indicates the corresponding pins that are shorted or closed.

Table 7. Jumper Settings and Functions (continued)

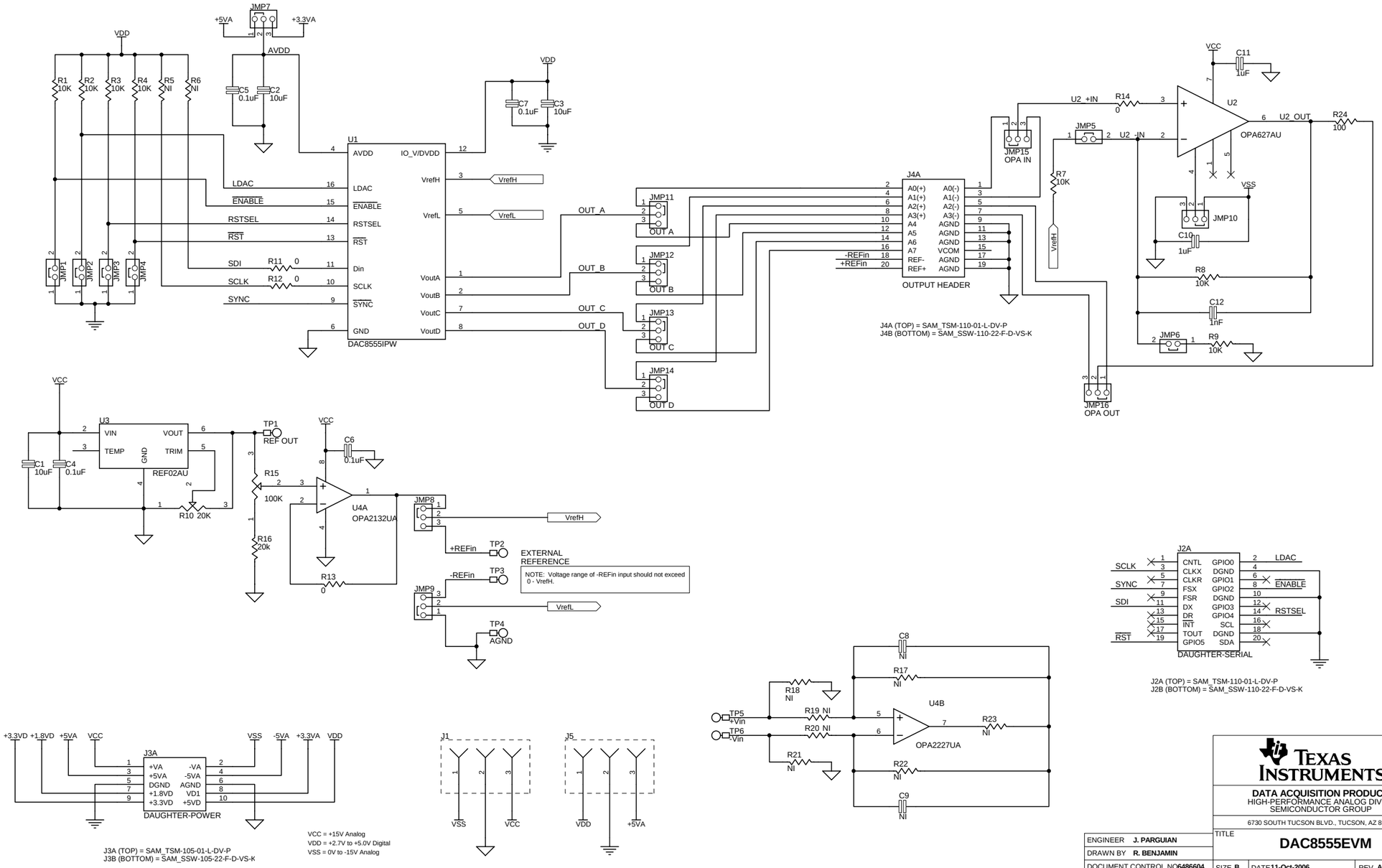
Reference	Jumper Setting[(1)]	Function
JMP4		$\overline{RST}$ pin is set high through pull-up resistor R4. $\overline{RST}$ can be driven by GPIO5, J2-19.
		$\overline{RST}$ pin is set low.
JMP5		Disconnects $V_{REF}H$ to the inverting input of the op amp U2.
		Connects $V_{REF}H$ to the inverting input of the op amp U2.
JMP6		Disconnects the inverting input of the op amp U2 from the gain resistor, R9.
		Connects the inverting input of the op amp U2 from the gain resistor, R9 for output gain of 2.
JMP7		+5V analog supply is selected for AV_{DD}.
		+3.3V analog supply is selected for AV_{DD}.
JMP8		Routes the adjustable, buffered, onboard +5V reference to the $V_{REF}H$ input of the DAC8555.
		Routes the user-supplied reference from TP2 or J4-20 to the $V_{REF}H$ input of the DAC8555.
JMP9		$V_{REF}L$ is tied to AGND.
		Routes the user-supplied negative reference from TP3 or J4-18 to the $V_{REF}L$ input of the DAC8555. This voltage should be within the range of 0V to $V_{REF}H$.
JMP10		Negative supply rail of the op amp U2 is powered by V_{SS} for bipolar operation.
		Negative supply rail of the op amp U2 is tied to AGND for unipolar operation.
JMP11		Routes $V_{OUT}A$ to J4-2.
		Routes $V_{OUT}A$ to J4-10.

Table 7. Jumper Settings and Functions (continued)

Reference	Jumper Setting[(1)]	Function
JMP12		Routes V_{OUT}B to J4-4.
		Routes V_{OUT}B to J4-12.
JMP13		Routes V_{OUT}C to J4-6.
		Routes V_{OUT}C to J4-14.
JMP14		Routes V_{OUT}D to J4-8.
		Routes V_{OUT}D to J4-16.
JMP15		Routes J4-1 to U2 noninverting input.
		Routes J4-3 to U2 noninverting input.
JMP16		Routes U2 output to J4-5.
		Routes U2 output to J4-7.

4 Schematic

REVISION HISTORY		
REV	ENGINEERING CHANGE NUMBER	APPROVED



TEXAS INSTRUMENTS

DATA ACQUISITION PRODUCTS
HIGH-PERFORMANCE ANALOG DIVISION
SEMICONDUCTOR GROUP

6730 SOUTH TUCSON BLVD., TUCSON, AZ 85706 USA

ENGINEER **J. PARGUIAN**	TITLE **DAC8555EVM**		
DRAWN BY **R. BENJAMIN**			
DOCUMENT CONTROL NO **6486604**	SIZE **B**	DATE **11-Oct-2006**	REV **A**
SHEET **1** OF **1**	FILE **C:\USERDATA\Projects\DAC8555\DAC8555EVM.ddb**		

FCC Warning

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general customer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

EVALUATION BOARD/KIT IMPORTANT NOTICE

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

This evaluation board/kit is intended for use for **ENGINEERING DEVELOPMENT, DEMONSTRATION, OR EVALUATION PURPOSES ONLY** and is not considered by TI to be a finished end-product fit for general consumer use. Persons handling the product(s) must have electronics training and observe good engineering practice standards. As such, the goods being provided are not intended to be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety and environmental measures typically found in end products that incorporate such semiconductor components or circuit boards. This evaluation board/kit does not fall within the scope of the European Union directives regarding electromagnetic compatibility, restricted substances (RoHS), recycling (WEEE), FCC, CE or UL, and therefore may not meet the technical requirements of these directives or other related directives.

Should this evaluation board/kit not meet the specifications indicated in the User's Guide, the board/kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods. Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

TI currently deals with a variety of customers for products, and therefore our arrangement with the user **is not exclusive.**

TI assumes **no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein.**

Please read the User's Guide and, specifically, the Warnings and Restrictions notice in the User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For additional information on TI's environmental and/or safety programs, please contact the TI application engineer or visit www.ti.com/esh.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used.

EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of–15.75V to +15.75V and the output voltage range of –15V to +15V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
Low Power Wireless	www.ti.com/lpw	Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265